E.G.S. PILLAY ENGINEERING COLLEGE

(An Autonomous Institution, Affiliated to Anna University, Chennai)
Nagore Post, Nagapattinam – 611 002, Tamilnadu.

Rev.0
COE/2017/QB

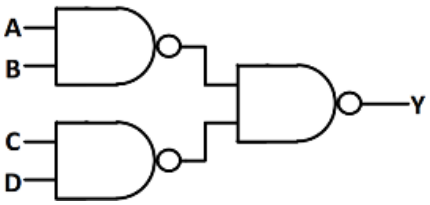
DIGITAL ELECTRONICS

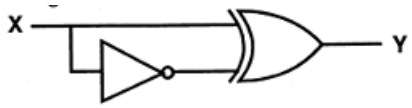
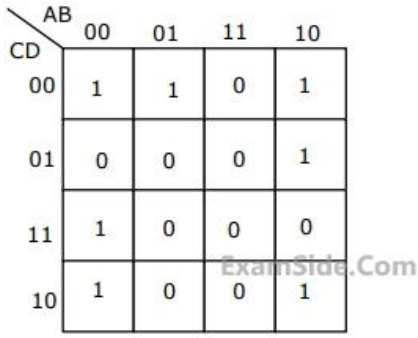
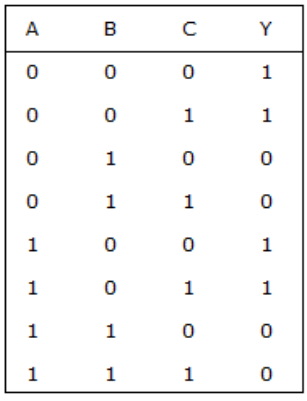
Academic Year :	2021-2022	**Question Bank**	Programme	B.E - EEE
Year / Semester :	II / III		Course Coordinator:	Dr. V.Mohan

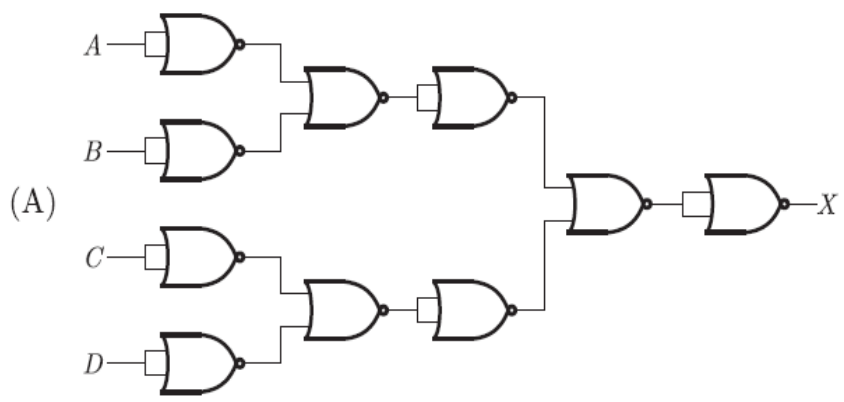
Course Objectives	Course Outcomes
1. To study the fundamentals of digital systems, programmable logic devices and logic families. 2. To design and implement combinational logic circuits. 3. To design and implement synchronous and asynchronous sequential logic circuits.	On the successful completion of the course, students will be able to CO1: Solve digital system problems using number systems, binary codes, logic gates, Boolean algebra and Karnaugh Map (K3) CO2: Construct combinational logic circuits using logic gates and multiplexers (K3) CO3: Build synchronous sequential logic circuits using excitation table, stable table and state diagrams (K3) CO4: Construct asynchronous sequential logic circuits using flow table, transition table, state assignment and state reduction techniques (K3) CO5: Implement Boolean functions and combinational logic circuits using memories, programmable logic devices and logic families (K3)

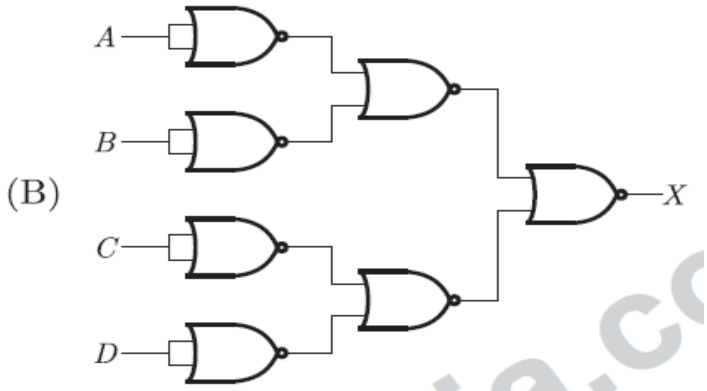
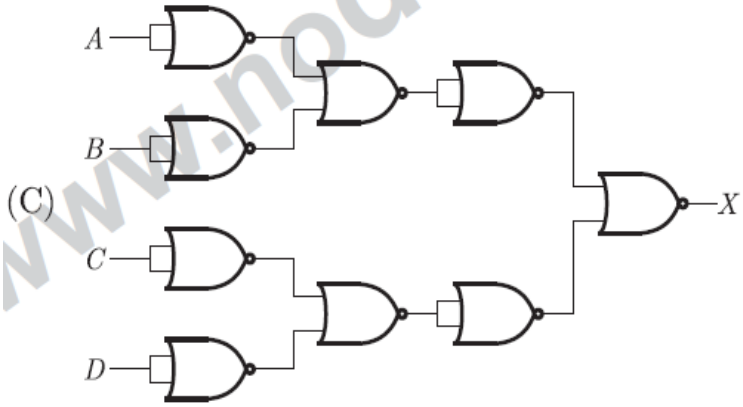
MODULE 1: NUMBER SYSTEM AND BOOLEAN ALGEBRA

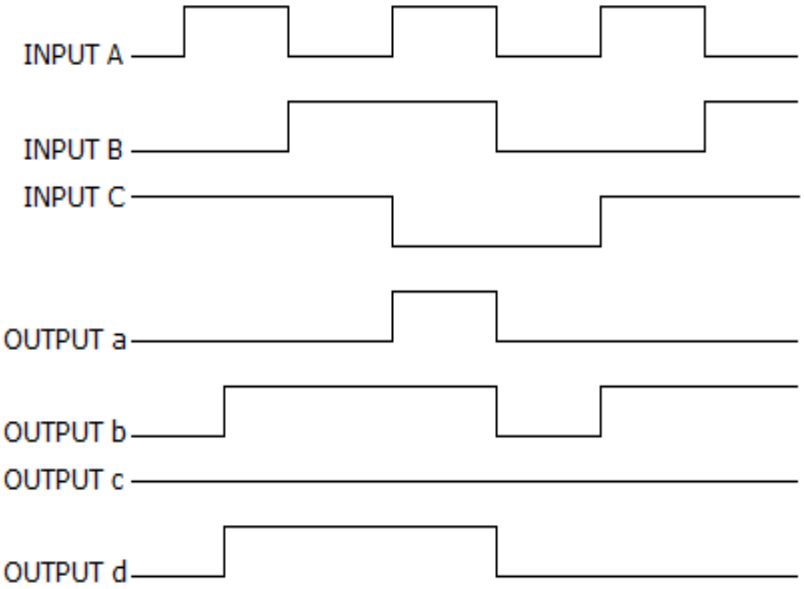
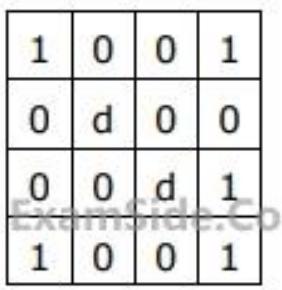
CO1: Solve digital system problems using number systems, binary codes, logic gates, Boolean algebra and Karnaugh Map (K3)

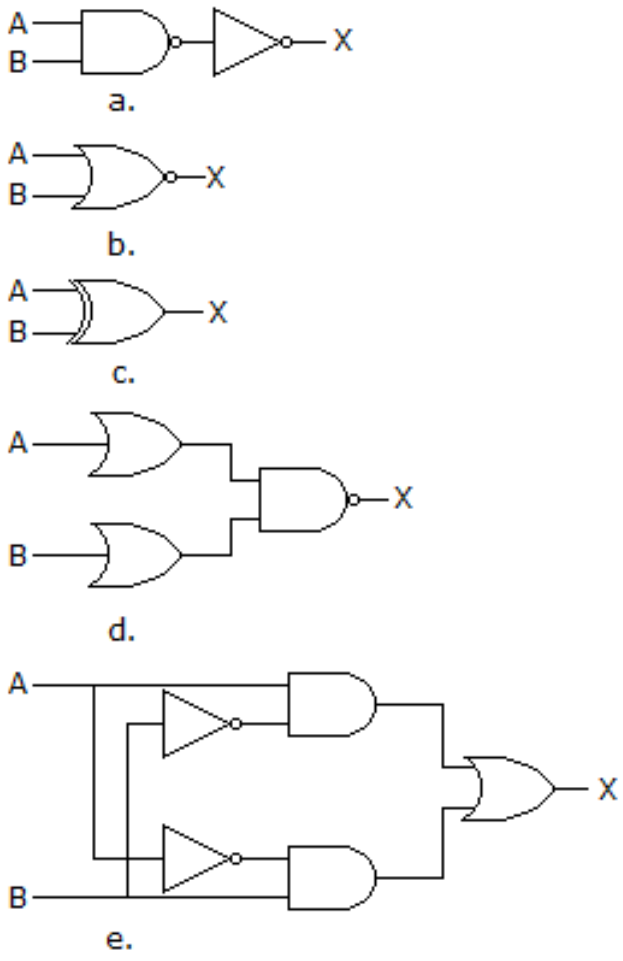
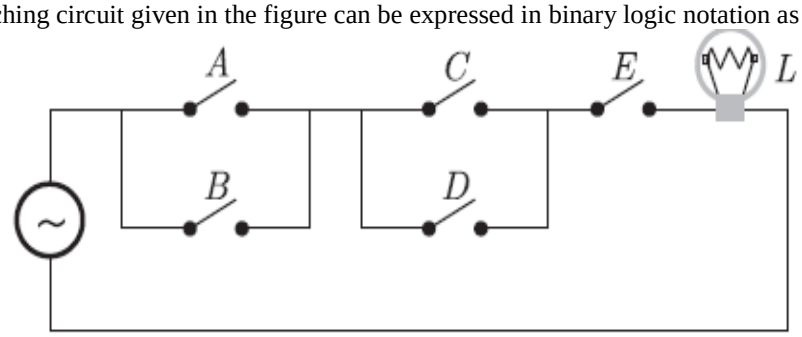
S.No	Questions	Mark	COs	BTL
1	For a 3-input NOR gate with eight input possibilities, how many of those possibilities will result in a HIGH output? **a) 1** b) 2 c) 7 d) 8	1	1	2
2	In the logic circuit shown in the figure, Y is given by  a) Y=ABCD b) Y=(A+B)(C+D) c) Y=A+B+C+D **d) Y=AB+CD**	1	1	3
3	The Gray code for decimal number 6 is equivalent to (A) 1100 (B) 1001 **(C) 0101** (D) 0110	1	1	2
4	The binary equivalent of FA_{16} is (A) 1010 1111	1	1	2

	(B) 1111 1010 (C) 10110011 (D) none of these			
5	How many two input AND gates and two input OR gates are required to realize Y = BD+CE+AB (A) 1, 1 (B) 4, 2 **(C) 3, 2** (D) 2, 3	1	1	3
6	The output Y of the logic circuit given below is  **a) 1** b) 0 c) X d) X’	1	1	2
7	The K-map for a Boolean function is shown in figure. The number of essential prime implicants for this function is  **(A) 4** (B) 5 (C) 6 (D) 8	1	1	3
8	For the given truth table, Y = …….  a) A + B + C b) A’+BC c) A’ **d) B’**	1	1	2

9	In a 7 segment LED display, identify the segments to be illuminated to display the decimal number 4? a) Segments a, f, b, c b) Segments c, d, e, f c) Segments a, d, e, g d) **Segments b, c, f, g**	1	1	2
10	Convert 59.72_{10} to BCD. a) 111011.1001000 **b) 01011001.01110010** c) 1011001.0111001 d) 0101100101110010	1	1	2
11	Convert $8B3F_{16}$ to binary. a) 35647 b) 011010 c) 1011001111100011 **d) 1000101100111111**	1	1	2
12	$(734)_8 = (\ )_{16}$ (A) C 1 D (B) D C 1 (C) 1 C D **(D) 1 D C**	1	1	2
13	2's complement of 11001011 is _____ a) 01010111 b) 11010100 **c) 00110101** d) 11100010	1	1	2
14	Add the two BCD numbers: 1001 + 0100 = ? a) 10101111 b) 01010000 **c) 00010011** d) 00101011	1	1	2
15	The excess-3 code for 597 is given by _____ **a) 100011001010** b) 100010100111 c) 010110010111 d) 010110101101	1	1	2
16	Select the circuit for the Boolean function X = (AB)' + (CD)'? (A) 	1	1	3

	  (D) None of the above **Answer: A**			
17	The expression Y=AB+BC+AC shows the _____ operation. a) EX-OR **b) SOP** c) POS d) NOR	1	1	2
18	Binary subtraction of 101101 – 001011 = ? **a) 100010** b) 010110 c) 110101 d) 101100	1	1	2
19	For a 3-input NAND gate, with the input waveforms as shown below, which output waveform is correct?	1	1	2

	 (A) a (B) b **(C) c** (D) d			
20	The number of product terms in the minimized sum-of-product expression obtained through the following k-map is (where , "d" denotes don't care states)  **a. 2** b. 3 c. 4 d. 5	1	1	3
21	The Boolean function Y= AB + CD is to be realized using only 2 input NAND gates. Calculate the minimum number of gates required. (a) 2 **(b) 3** (c) 4 (d) 5	1	1	3
22	For the identity, AB+A'C+BC=AB+A'C, the dual form is	1	1	2

	(a) $(A+B)(\bar{A}+C)(B+C)=(A+B)(\bar{A}+C)$ (b) $(\bar{A}+\bar{B})(A+\bar{C})(\bar{B}+\bar{C})=(\bar{A}+\bar{B})(A+\bar{C})$ (c) $(A+B)(\bar{A}+C)(B+C)=(\bar{A}+\bar{B})(A+\bar{C})$ (d) $\bar{A}\,\bar{B}+A\,\bar{C}+\bar{B}\,\bar{C}=\bar{A}\,\bar{B}+A\,\bar{C}$ **Answer: a**			
23	Which of the figures in figure (a to d) is equivalent to figure (e)?  a. a b. b **c. c** d. d	1	1	2
24	The switching circuit given in the figure can be expressed in binary logic notation as  	1	1	3

(A) $L = (A + B)(C + D)E$

(B) $L = AB + CD + E$

(C) $L = E + (A + B)(C + D)$

(D) $L = (AB + CD)E$

Answer: A

25 From the truth table below, determine the standard SOP expression. 1 1 3

Inputs			Output
A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

(A) $X = \overline{A}\,\overline{B}\,\overline{C} + A\,B\,C + A\,\overline{B}\,C$

(B) $X = A\,B\,C + A\,B\,C + A\,B\,C$

(C) $X = A\,\overline{B}\,C + \overline{A}\,B\,C + A\,B\,\overline{C}$

(D) $X = \overline{A}\,\overline{B}\,C + \overline{A}\,B\,C + A\,B\,\overline{C}$

Answer: D

26 Match the following: 2 1 1

List – I		List – II
a.	Controlled Inverter	i. a circuit that can add 3 bits
b.	Full adder	ii. a circuit that can add two binary numbers
c.	Half adder	iii. a circuit that transmits a binary word or its 1's complement
d.	Binary adder	iv. a logic circuit that adds 2 bits

Codes :

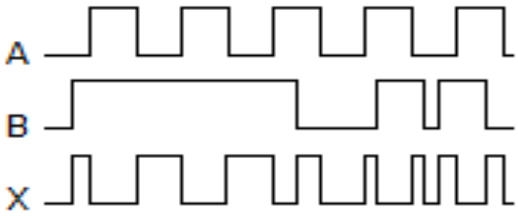
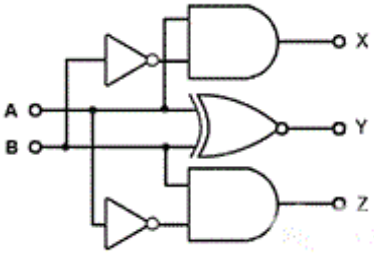
	a	b	c	d
(1)	iii	ii	iv	i
(2)	ii	iv	i	iii
(3)	iii	iv	i	ii
(4)	iii	i	iv	ii

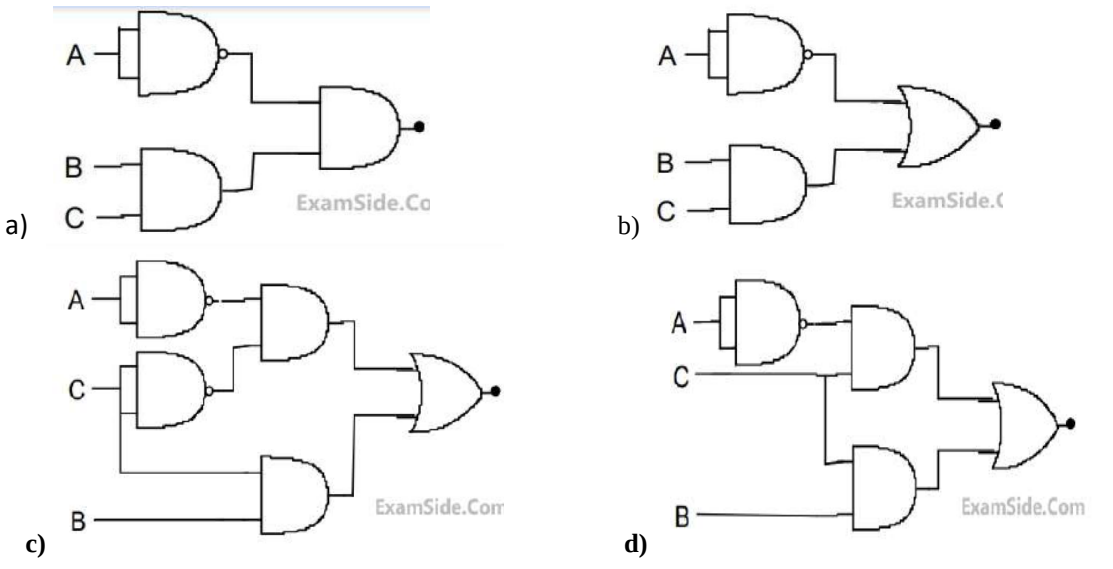
a) 1

b) 2

c) 3

d) 4

27	The simplification of the Boolean expression $(\overline{A}\overline{B}\overline{C})+(A\overline{B}\overline{C})$ (A) 0 **(B) 1** (C) A (D) BC	2	1	3
28	Perform multiplication of the binary numbers: 01001 × 01011 = ? a) **001100011** b) 110011100 c) 010100110 d) 101010111	2	1	2
29	In a natural food restaurant, fruit is offered for desert but only in certain combination. One choice is either orange or apple or both. Another choice is either mango and apple or neither. A third choice is orange, but if you choose orange, then you must also take banana. The fruits are represented by their first alphabet of the name. Make use of Boolean logic, represent the fruit available for desert in simplified form. a) A + B b) M + O **c) A + O** d) M + B	2	1	3
30	The following waveform pattern is for _____.  a) 2-input AND gate b) 2-input OR gate **c) Exclusive-OR gate** d) None of the above	2	1	3
31	Digital input signals A,B,C with A as the MSB and C as the LSB are used to realize the Boolean function $F=m_0+m_2+m_3+m_5+m_7$ where m_i denotes the i^{th} minterm. In addition, F has don't care for m_1. The simplified expression for F is given by a) A'C'+B'C+AC **b) A'+C** c) C'+A d) A'C+BC+AC'	2	1	3
32	In the given logic circuit the inputs are A = 0 and B = 1. Identify the logic states at X, Y and Z.  	2	1	3

	a) X=1, Y=1, Z=0 b) X=1, Y=0, Z=0 c) X=0, Y=1, Z=0 **d) X=0, Y=0, Z=1**			
33	Make use of Karnaugh map reduction technique, find the output expression BC A \ 00 01 11 10 0 1 0 0 1 1 1 1 1 1 a) A+B' **b) A+C'** c) A'+C' d) A'+C	2	1	3
34	The elevator door should open if the elevator is stopped, it is level with the floor and the timer has not expired, or if the elevator is stopped, it is level with the floor, and a button is pressed. If D = elevator door opens; S = elevator is stopped; F = level with floor; T = timer expired and B = button pressed, select the Boolean expression that satisfies the above condition. **a) D = SFT' + SFB** b) D = SFT'B c) D = SF + T'B d) D = (S+F) T' B	2	1	3
35	Identify the logic circuit that realizes the function F whose Karnaugh map is shown in figure. AB C \ 00 01 11 10 0 1 1 C 1 1 1  **Answer: C**	2	1	3