

E.G.S. PILLAY ENGINEERING COLLEGE

(An Autonomous Institution, Affiliated to Anna University, Chennai) Nagore Post, Nagapattinam – 611 002, Tamilnadu. Rev.0 COE/2017/QB

DIGITAL ELECTRONICS								
Academic Year : 2021-2022			2021-2022	Question Bank	Programme	B.E - EEE		
Year /	Semester	:	II / III	Question Dank	Course Coordinator:	Dr. V.Mohan		
Course Objectives			ctives		Course Outcomes			
 To di lo, To co To sy se 	 To study the fundamentals of digital systems, programmable logic devices and logic families. To design and implement combinational logic circuits. To design and implement synchronous and asynchronous sequential logic circuits. 			 On the successful completion of the course, students will be able to CO1: Solve digital system problems using number systems, binary codes, logic gates, Boolean algebra and Karnaugh Map (K3) CO2: Construct combinational logic circuits using logic gates and multiplexers (K3) CO3: Build synchronous sequential logic circuits using excitation table, stable table and state diagrams (K3) CO4: Construct asynchronous sequential logic circuits using flow table, transition table, state assignment and state reduction techniques (K3) CO5: Implement Boolean functions and combinational logic circuits using memories, programmable logic devices and logic families (K3) 				
CO2: 0	Construct	combin	ational logic circ	cuits using logic gates and multiplexe	ers (K3)			
S.No				Questions		Mark	COs	BTL
1	a) b) c) d)	Compara Multiple Demulti Parity ge	ator e xer plexer enerator	ely a D_0 D_1 D_2 D_3 S_0 S_1 \overline{EN}			2	2
2	For the d What is t	evice she	own here, let all I s of the Y output?	D inputs be LOW, both S inputs be HI D_0 D_1 D_2 D_3 S_0 S_1 \overline{EN} \longrightarrow	GH, and the EN input be LOV	W. 1	2	2

	A. LOW			
	B. HIGH			
	D. Cannot be determined			
3	A multiplexer with a 4-bit data select input is a	1	2	2
	a) 4:1 multiplexer b) 2:1 multiplexer			
	c) 16:1 multiplexer			
	d) 8:1 multiplexer			
4	A combinational logic circuit is shown here. It has 3 inputs A, B, C and 2 outputs D, E. Identify the name of the circuit.	1	2	2
	 a) full adder b) full subtractor c) shift register 			
	d) decade counter			
5	Match the terms in List - I with the options given in List - II :	1	2	2
	List - IList - II(a) Decoder(i) 1 line to 2^n lines(b) Multiplexer(ii) n lines to 2^n lines(c) De multiplexer(iii) 2^n lines to 1 line(iv) 2^n lines to 2^{n-1} lines			
	codes:			
	(a) (b) (c)			
	(1) (ii) (i) (iii)			
	(2) (ii) (iii) (i)			
	(3) (ii) (i) (iv)			
	$ \begin{array}{cccc} (4) & (iv) & (ii) & (i) \\ a) & (1) \\ b) & (2) \end{array} $			
	c) (3) (4)			
6	a) (4) Consider the two cascaded 2-to-1 multiplexers as shown in the figure	1	2	3
0	Consider the two case add 2-to-1 multiplexers as shown in the figure. $ \begin{array}{c} & \overline{R} \\ & 0 \\ & 0 \\ & 0 \\ & 2-to-1 \\ & 1 \\ & MUX \\ & s \\ & 1 \\ & P \\ & 0 \\ & 0 \\ & 1 \\ & MUX \\ & s \\ & 0 \\ &$	1	2	5
	Determine the minimal sum of products form of the output X.			

	(A) $\bar{P}\bar{Q} + PQR$			
	(B) $\bar{P}Q + QR$			
	(C) $PQ + \bar{P}\bar{Q}R$			
	(D) $\bar{Q}\bar{R} + PQR$			
	a) A			
	b) B c) C			
	d) D			
7	The device shown here is most likely a	1	2	2
	a) Comparator b) Multiplexer c) Inverter			
	d) Demultiplexer			
8	The design of an ALU is based on	1	2	1
	 a) Sequential logic b) Combinational logic c) Multiplexing d) De-Multiplexing 			
9	One that is not the outcome of magnitude comparator is	1	2	2
	a) a>b b) a-b c) a <b d) a=b</b 			
10	Procedure for the design of combinational circuits are: A. From the word description of the problem, identify the inputs and outputs and draw a block diagram.	1	2	2
	B. Draw the truth table such that it completely describes the operation of the circuit for different combinations of inputs.			
	C. Simplify the switching expression(s) for the output(s).			
	E. Write down the switching expression(s) for the output(s).			
	a) B, C, D, E, A b) A, D, E, B, C c) A, B, E, C, D d) B, A, E, C, D			
11	The number of control lines for 32 to 1 multiplexer is	1	2	2
	a) 4 b) 5 c) 16 d) 6			

12	The number of bits in nibble and byte are and respectively.	1	2	1
	a) $2, 8$ b) 816			
	c) 4,8			
	d) 1,4			
13	Which of the following is not a combinational logic circuit?	1	2	2
	a) Full adder			
	b) Encoder			
	c) Counter			
	d) Demultiplexer			
14	A device which converts decimal number into BCD form is called and the device which converts BCD	1	2	1
	into octal is called			
	a) Encoder. Decoder			
	b) Decoder, Encoder			
	c) code converter, demultiplexer			
15	d) multiplexer, Decoder The automative of a 2 hit and an angle of a link and a link and the 2 hit input D. The	1	2	2
15	The output Y of a 2 bit comparator is logic 1 whenever the 2-bit input A is greater than the 2-bit input B. The number of combination for which the output is logic 1 is	1	2	3
	number of combination for which the output is logic 1, is			
	a) 4			
	b) 6			
	c) 8 d) 10			
16	d) 10 How many select lines would be required for an 8-line-to-1-line multiplexer?	1	2	2
10	now many select miles would be required for an o mile to 1 mile manuplexer.	1	-	2
	a) 2			
	b) 4			
	c) 8			
17	In the given 4-to-1 multiplexer, if $c_1 = 0$ and $c_0 = 1$ then the output M is	1	2	2
- /		1	_	_
	c_1 c_0			
	X ₂			
	X ₃			
	a) X0			
	b) X1			
	c) X_2			
18	If we record any music in any recorder, such types of process is called	1	2	2
		-		
	a) Multiplexing			
	b) Encoding			
	d) Demultiplexing			
	o, 2 chieft proving			

19	A certain BCD-to-decimal decoder has active-HIGH inputs and active-LOW outputs. Which output goes	1	2	2
	LOw when the inputs are 1001?			
	A. 0			
	B. 3			
	C. 9 D None All outputs are HIGH			
20	A basic multiplexer principle can be demonstrated through the use of a	1	2	2
	a) Single-pole relay			
	b) DPDT switch			
	c) Rotary switch d) Linear stepper			
21	How many select lines would be required for an 8-line-to-1-line multiplexer?	1	2	2
	a) 2			
	b) 4			
	d) 5			
22	A combinational circuit which is used to send data coming from a single source to two or more separate	1	2	1
	destinations is called as:			
	(a) Decoder b) Encoder			
	c) Multiplexer			
	d) Demultiplexer			
22	The simulified supression of full odden compris	1	2	2
25	The simplified expression of run adder carry is	1	Z	Z
	a) $c = xy + xz + yz$			
	b) $c = xy + xz$			
	c) $c = xy+yz$			
	d = x + y + z			
24	In a combinational circuit, the output at any time depends only on the at that time.	1	2	1
	a) Past output values			
	b) Intermediate values			
	c) Both past output and present input			
	d) Present input values			
25	Which one of the following is odd?	1	2	2
	a) Multipleyer			
	b) Decoder			
	c) Adder			
	d) Flip-Flop			
26	In the following circuit, the motor will turn on when $DRIVE = 1$	2	2	3
-		-	-	







