	E.G.S. PILLAY ENGINEERING COLLEGE (An Autonomous Institution, Affiliated to Anna University, Chennai) Nagore Post, Nagapattinam – 611 002, Tamilnadu.	Rev.0 COE/2017/QB

DIGITAL ELECTRONICS

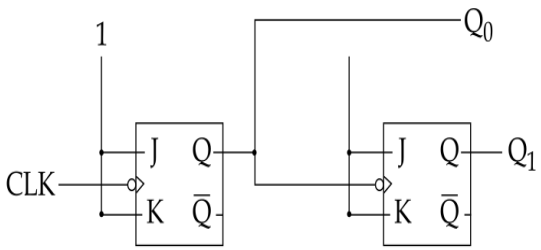
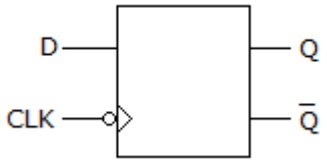
Academic Year :	2021-2022	**Question Bank**	Programme	B.E - EEE
Year / Semester :	II / III		Course Coordinator:	Dr. V.Mohan

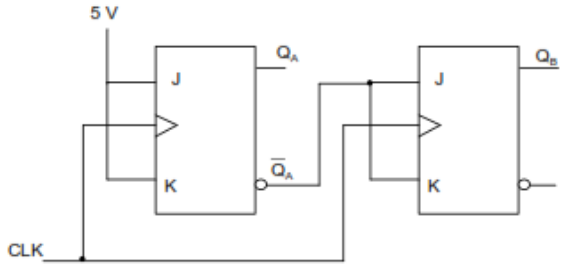
Course Objectives	Course Outcomes
1. To study the fundamentals of digital systems, programmable logic devices and logic families. 2. To design and implement combinational logic circuits. 3. To design and implement synchronous and asynchronous sequential logic circuits.	On the successful completion of the course, students will be able to CO1: Solve digital system problems using number systems, binary codes, logic gates, Boolean algebra and Karnaugh Map (K3) CO2: Construct combinational logic circuits using logic gates and multiplexers (K3) CO3: Build synchronous sequential logic circuits using excitation table, stable table and state diagrams (K3) CO4: Construct asynchronous sequential logic circuits using flow table, transition table, state assignment and state reduction techniques (K3) CO5: Implement Boolean functions and combinational logic circuits using memories, programmable logic devices and logic families (K3)

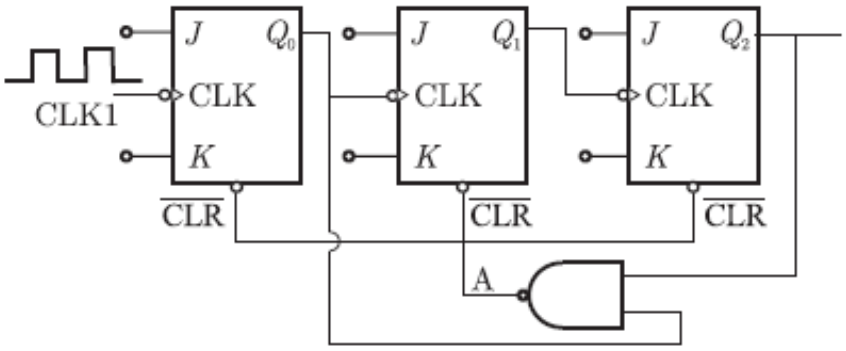
MODULE 3: SYNCHRONOUS SEQUENTIAL LOGIC CIRCUITS

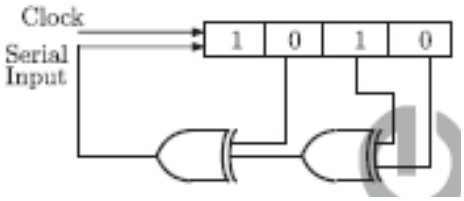
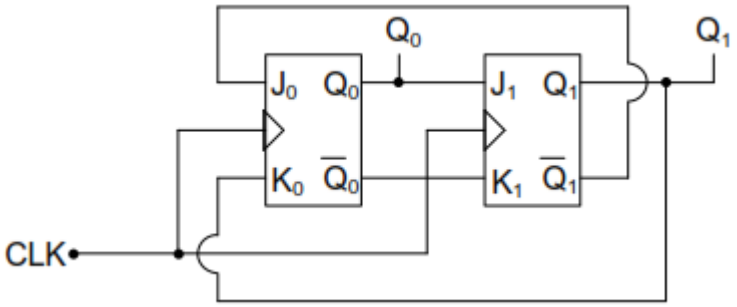
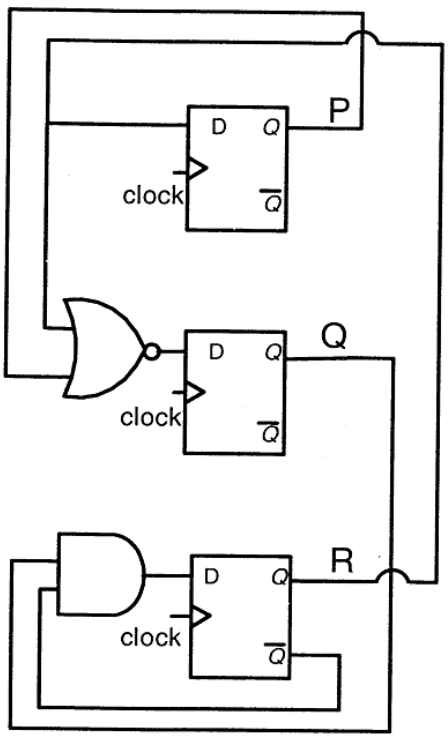
CO3: Build synchronous sequential logic circuits using excitation table, stable table and state diagrams (K3)

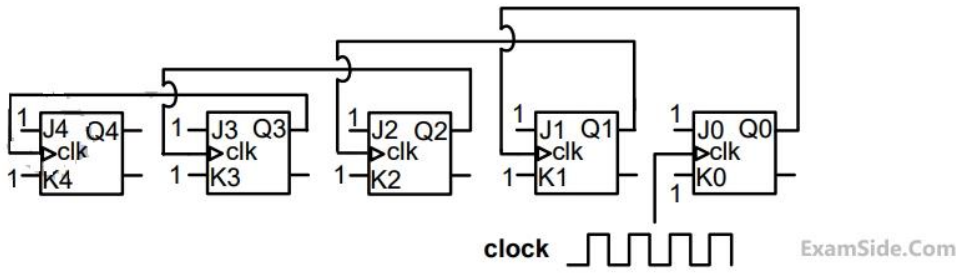
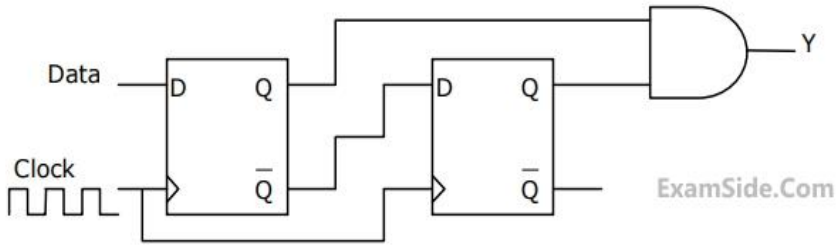
S.No	Questions	Mark	COs	BTL
1	The minimum number of flip-flops needed to construct a BCD decade counter is **a) 4** b) 3 c) 10 d) 2	1	3	2
2	The terminal count of a modulus-11 binary counter is _____. **a) 1010** b) 1000 c) 1001 d) 1100	1	3	2
3	If the input to T-flipflop is 100 Hz signal, the final output of the three T-flipflops in cascade is (A) 1000 Hz (B) 500 Hz (C) 333 Hz **(D) 12.5 Hz**	1	3	2
4	A cascade of three identical modulo-5 counters has an overall modulus of (A) 5 (B) 25 **(C) 125** (D) 625	1	3	2
5	Which of the following is a sequential circuit? a) Multiplexer b) Decoder **c) Counter** d) Full adder	1	3	1

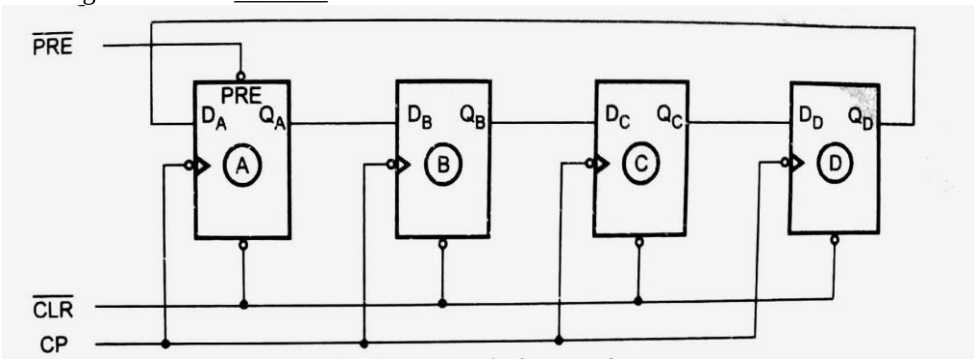
6	What does the following logic diagram represent?  a) Synchronous Counter **b) Ripple Counter** c) Combinational Circuit **d)** Mod 2 Counter	1	3	2
7	A 4-bit synchronous counter uses flip-flops with propagation delay times of 15 ns each. The maximum possible time required for change of state will be **(A) 15 ns** (B) 30 ns (C) 45 ns (D) 60 ns	1	3	2
8	On a J-K flip-flop, when is the flip-flop in a hold condition? **a) J = 0, K = 0** b) J = 1, K = 0 c) J = 0, K = 1 d) J = 1, K = 1	1	3	2
9	What does the circle on the clock input of a J-K flip-flop mean? a) Level enabled b) Positive edge triggered **c) negative edge triggered** d) Level triggered	1	3	1
10	The term synchronous means _____ a) The output changes state only when any of the input is triggered **b) The output changes state only when the clock input is triggered** c) The output changes state only when the input is reversed d) The output changes state only when the input follows it	1	3	1
11	What is the maximum possible range of bit-count specifically in n-bit binary counter consisting of 'n' number of flip-flops? a) 0 to 2^n b) 0 to $2^n + 1$ c**) 0 to $2^n - 1$** d) 0 to $2^{n+1/2}$	1	3	2
12	The symbols on this flip-flop device indicate _____.  **A. triggering takes place on the negative-going edge of the CLK pulse** B. triggering takes place on the positive-going edge of the CLK pulse C. triggering can take place anytime during the HIGH level of the CLK waveform D. triggering can take place anytime during the LOW level of the CLK waveform	1	3	2
13	What is one disadvantage of an S-R flip-flop?	1	3	1

	A. It has no enable input. **B. It has an invalid state.** C. It has no clock input. D. It has only a single output.			
14	What is the difference between a ring shift counter and a Johnson shift counter? A. There is no difference. B. A ring is faster. **C. The feedback is reversed.** D. The Johnson is faster.	1	3	1
15	A ring counter consisting of five Flip-Flops will have **(A) 5 states** (B) 10 states (C) 32 states (D) Infinite states.	1	3	2
16	A positive edge-triggered D flip-flop will store a 1 when _____ a) The D input is HIGH and the clock transitions from HIGH to LOW **b) The D input is HIGH and the clock transitions from LOW to HIGH** c) The D input is HIGH and the clock is LOW d) The D input is HIGH and the clock is HIGH	1	3	2
17	To operate correctly, starting a ring shift counter requires: A. clearing all the flip-flops **B. presetting one flip-flop and clearing all others** C. clearing one flip-flop and presetting all others D. presetting all the flip-flops	1	3	2
18	Ripple counters are also called _____ a) SSI counters **b) Asynchronous counters** c) Synchronous counters d) VLSI counters	1	3	1
19	The current state Q_A Q_B of a two JK flip-flop system is 00. Assume that the clock rise-time is much smaller than the delay of the JK flip-flop. The next state of the system is  (A) 00 (B) 01 **(C) 11** (D) 10	1	3	3
20	Assume a 4-bit ripple counter has a failure in the second flip-flop such that it “locks up”. The third and fourth stages will _____ a) Continue to count with correct outputs b) Continue to count but have incorrect outputs **c) Stop counting** d) Turn into molten silicon	1	3	2
21	If a 10-bit ring counter has an initial state 1101000000, what is the state after the second clock pulse? a) 1101000000 **b) 0011010000** c) 1100000000 d) 0000000000	1	3	2

22	In a 4-bit Johnson counter sequence, there are a total of how many states, or bit patterns? a) 1 b) 3 c) 4 **d) 8**	1	3	2
23	High speed counter is _____ a) Ring counter b) Ripple counter **c) Synchronous counter** d) Asynchronous counter	1	3	1
24	A flip-flop can be constructed with two NAND gates or with _____ a) Two AND gates b) Two OR gates **c) Two NOR gates** d) Two NOT gates	1	3	1
25	What is the function of a buffer circuit? A. to provide an output that is inverted from that on the input **B. to provide an output that is equal to its input** C. to clean up the input D. to clean up the output	1	3	1
26	The ripple counter shown in figure is made up of negative edge triggered J-K flip-flops. The signal levels at J and K inputs of all the flip flops are maintained at logic 1. Assume all the outputs are cleared just prior to applying the clock signal. The module no. of the counter is:  (A) 7 (B) 5 (C) **4** (D) 8	2	3	3
27	An eight stage ripple counter uses a flip-flop with propagation delay of 75 nanoseconds. The pulse width of the strobe is 50ns. The frequency of the input signal which can be used for proper operation of the counter is approximately. **(A) 1 MHz** (B) 500 MHz (C) 2 MHz (D) 4 MHz	2	3	3
28	The shift register shown in figure is initially loaded with the bit pattern 1010. Subsequently the shift register is clocked, and with each clock pulse the pattern gets shifted by one bit position to the right. With each shift, the bit at the serial input is pushed to the left most position (msb). After how many clock pulses will the content of the shift register become 1010 again?	2	3	3

	 (A) 3 **(B) 7** (C) 11 (D) 15			
29	In the following sequential circuit, the initial state (before the first clock pulse) of the circuit is Q_1Q_0= 00. The state (Q_1Q_0), immediately after the 3rd clock pulse is  (A) 00 **(B) 01** (C) 10 (D) 11	2	3	3
30	Consider the following circuit involving three D-type flip-flops used in a certain type of counter configuration.  If at some instance prior to the occurrence of the clock edge, P, Q and R have a value 0, 1 and 0 respectively, what shall be the value of PQR after the clock edge? (A) 000 (B) 001 (C) 010 **(D) 011**	2	3	3

31	A 12 MHz clock frequency is applied to a cascaded counter containing a modulus-5 counter, a modulus-8 counter, and a modulus-10 counter. The lowest output frequency possible is _____ a) 10 kHz b) 20 kHz **c) 30 kHz** d) 60 kHz	2	3	3
32	Choose the correct one from among the alternatives A, B, C, D after matching an item from Group 1 with the most appropriate item in Group 2. Group1 P. shift register Q. Counter R. Decoder Group2 1. Frequency division 2. Addressing in memory chips 3. Serial to parallel data conversion A P-3, Q-2, R-1 B P-3, Q-1, R-2 C P-2, Q-1, R-3 D P-1, Q-3, R-2 **Answer: B**	2	3	2
33	Five JK flip - flops are cascaded to form circuit shown in figure. Clock pulses at a frequency of 1 MHz are applied as shown. The frequency (in kHz) of the waveform at Q_3 is _____.  a) 500 kHz **b) 62.5 kHz** c) 250 kHz d) 125 kHz	2	3	3
34	When the output Y in the circuit below is '1', it implies that data has  **a) Changed from 0 to 1** b) Changed from 1 to 0 c) Not changed d) Changed in either direction	2	3	3

35	The name of the gien circuit is _____  a) Jhonson counter b) Up counter **c) Ring counter** **d)** Don counter	2	3	2