	E.G.S. PILLAY ENGINEERING COLLEGE (An Autonomous Institution, Affiliated to Anna University, Chennai) Nagore Post, Nagapattinam – 611 002, Tamilnadu.	Rev.0 COE/2017/QB

DIGITAL ELECTRONICS

Academic Year :	2021-2022	**Question Bank**	Programme	B.E - EEE
Year / Semester :	II / III		Course Coordinator:	Dr. V.Mohan

Course Objectives	Course Outcomes
1. To study the fundamentals of digital systems, programmable logic devices and logic families. 2. To design and implement combinational logic circuits. 3. To design and implement synchronous and asynchronous sequential logic circuits.	On the successful completion of the course, students will be able to CO1: Solve digital system problems using number systems, binary codes, logic gates, Boolean algebra and Karnaugh Map (K3) CO2: Construct combinational logic circuits using logic gates and multiplexers (K3) CO3: Build synchronous sequential logic circuits using excitation table, stable table and state diagrams (K3) CO4: Construct asynchronous sequential logic circuits using flow table, transition table, state assignment and state reduction techniques (K3) CO5: Implement Boolean functions and combinational logic circuits using memories, programmable logic devices and logic families (K3)

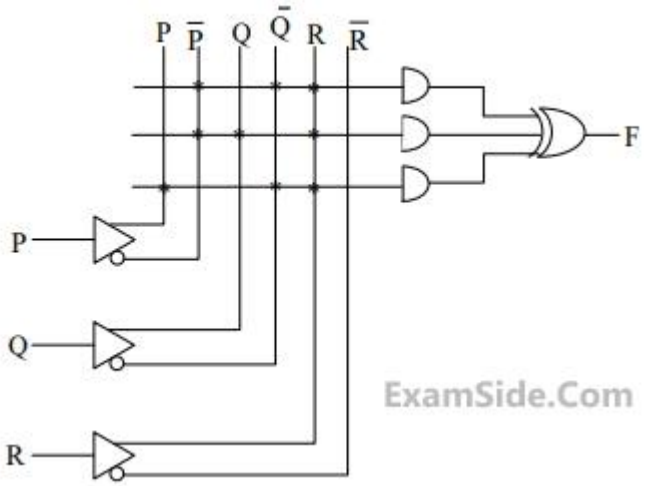
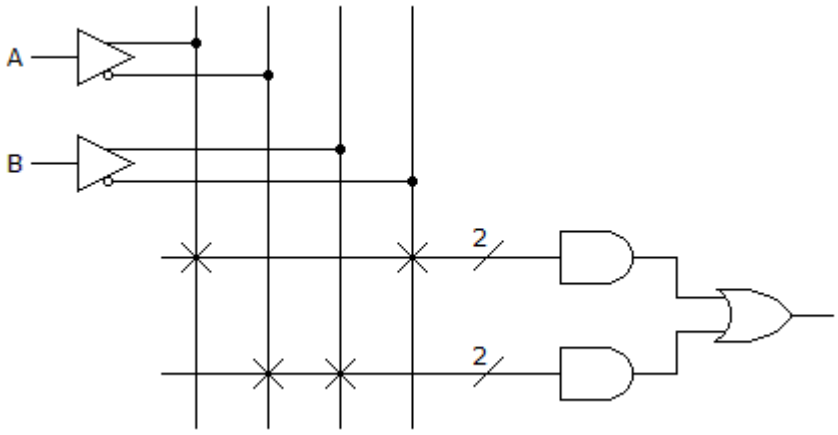
MODULE 5: MEMORY DEVICES, PROGRAMMABLE LOGIC DEVICES AND LOGIC FAMILIES

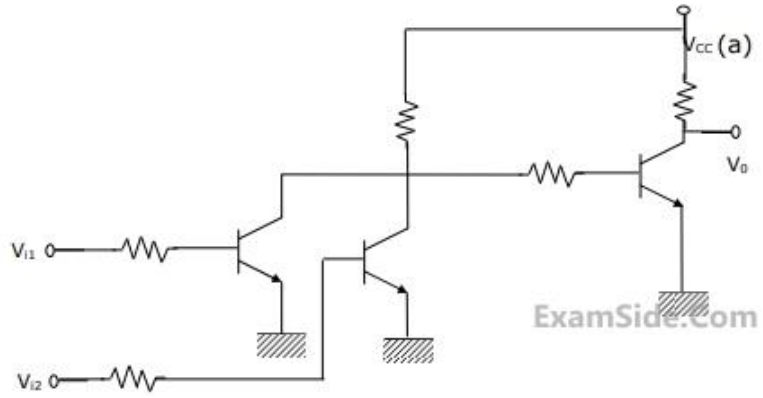
CO5: Implement Boolean functions and combinational logic circuits using memories, programmable logic devices and logic families (K3)

S.No	Questions	Mark	COs	BTL
1	PLDs with programmable AND and fixed OR arrays are called _____ **a) PAL** b) PLA c) APL d) PPL	1	5	1
2	When both the AND and OR are programmable, such PLDs are known as _____ a) PAL b) PPL **c) PLA** d) APL	1	5	1
3	The full form of EEPROM is _____ a) Erasable Electrically Programmable ROMs **b) Electrically Erasable Programmable ROMs** c) Electrically Erasable Programming ROMs d) Electrically Erasable Programmed ROMs	1	5	1
4	PLA is used to implement _____ a) A complex sequential circuit b) A simple sequential circuit **c) A complex combinational circuit** d) A simple combinational circuit	1	5	1
5	The digital logic family which has the lowest propagation delay time is **(A) ECL** (B) TTL (C) CMOS (D) PMOS	1	5	1
6	Which of the memory is volatile memory	1	5	1

	(A) ROM **(B) RAM** (C) PROM (D) EEPROM			
7	EPROM contents can be erased by exposing it to **a) Ultraviolet rays.** b) Infrared rays. c) Burst of microwaves. d) Intense heat radiations.	1	5	1
8	The inputs in the PLD is given through _____ a) NAND gates b) OR gates c) NOR gates **d) AND gates**	1	5	1
9	The difference between a PAL & a PLA is _____ a) PALs and PLAs are the same thing **b) The PLA has a programmable OR plane and a programmable AND plane, while the PAL only has a programmable AND plane** c) The PAL has a programmable OR plane and a programmable AND plane, while the PLA only has a programmable AND plane d) The PAL has more possible product terms than the PLA	1	5	2
10	Which family of devices has the characteristic of preventing saturation during operation? A. TTL B. MOS **C. ECL** D. IIL	1	5	1
11	Which of the following is the fastest logic? (A) TTL **(B) ECL** (C) CMOS (D) LSI	1	5	1
12	Which type of unipolar logic family exhibits its usability for the applications requiring low power consumption? a. PMOS b. NMOS **c. CMOS** d. All of the above	1	5	1
13	CMOS refers to _____. a) Continuous Metal Oxide Semiconductor **b) Complementary Metal Oxide Semiconductor** c) Centred Metal Oxide Semiconductor d) Concrete Metal Oxide Semiconductor	1	5	1
14	Fan-in is defined as _____ a) the number of outputs connected to gate without any degradation in the voltage levels **b) the number of inputs connected to gate without any degradation in the voltage levels** c) the number of outputs connected to gate with degradation in the voltage levels d) the number of inputs connected to gate with degradation in the voltage levels	1	5	1
15	Fan-in and Fan-out are the characteristics of _____. a) Registers **b) Logic families** c) Sequential Circuits d) Combinational Circuits	1	5	1
16	A 64-bit word consists of _____.	1	5	1

	A. 4 bytes **B. 8 bytes** C. 10 bytes D. 12 bytes			
17	Select the statement that best describes Read-Only Memory (ROM). A. nonvolatile, used to store information that changes during system operation **B. nonvolatile, used to store information that does not change during system operation** C. volatile, used to store information that changes during system operation D. volatile, used to store information that does not change during system operation	1	5	1
18	How many 2K × 8 ROM chips would be required to build a 16K × 8 memory system? A. 2 B. 4 **C. 8** D. 16	1	5	2
19	How many storage locations are available when a memory device has 12 address lines? A. 144 B. 512 C. 2048 **D. 4096**	1	5	2
20	Which is the most commonly used logic family a. ECL **b. TTL** c. CMOS d. PMOS	1	5	1
21	TTL uses **a. Multi emitter transistor** b. Multi collector transistor c. Multi base transistor d. Multi emitter or multi collector transistor	1	5	1
22	How many address bits are required to represent a 32 K memory? (A) 10 bits. (B) 12 bits. (C) 14 bits. **(D) 16 bits.**	1	5	2
23	Which of the following memories stores the most number of bits? **(A) a 5M X 8 memory.** (B) a 1M X16 memory. (C) a 5M X4 memory. (D) a 1M X12 memory.	1	5	2
24	Select the best description of the fusible-link PROM. 1. user programmable, reprogrammable **2. user programmable, one-time programmable** 3. manufacturer programmable, one-time programmable 4. manufacturer programmable, reprogrammable	1	5	2
25	Which of the following logic family has the complementary outputs? a) RTL b) DTL **c) ECL** d) TTL	1	5	1
26	A programmable logic array (PLA) is shown in the figure. The Boolean function F implemented is _____.	2	5	3

	 A $\overline{P}\,\overline{Q}\,R + \overline{P}QR + P\overline{Q}\,\overline{R}$ B $(\overline{P} + \overline{Q} + R)(\overline{P} + Q + R) + (P + \overline{P} + \overline{R})$ C $\overline{P}\,\overline{Q}\,R + \overline{P}QR + P\overline{Q}\,\overline{R}$ D $(\overline{P} + \overline{Q} + R)(\overline{P} + Q + R) + (P + \overline{Q} + R)$ **Answer: C**			
27	How many 16K * 4 RAMs are required to achieve a memory with a capacity of 64K and a word length of 8 bits? a) 2 b) 4 c) 6 **d) 8**	2	5	3
28	Which is the correct logic function for this PAL diagram?  (A) $X = \overline{A}\,\overline{B} + \overline{B}\,\overline{A}$ (B) $X = A\,\overline{B} + \overline{B}\,A$ (C) $X = A\,\overline{B} + B\,\overline{A}$ (D) $X = AB + BA$ **Answer: C**	2	5	3
29	The figure shows the circuit of a gate in the Resistor Transistor Logic (RTL) family. The circuit represents a	2	5	3



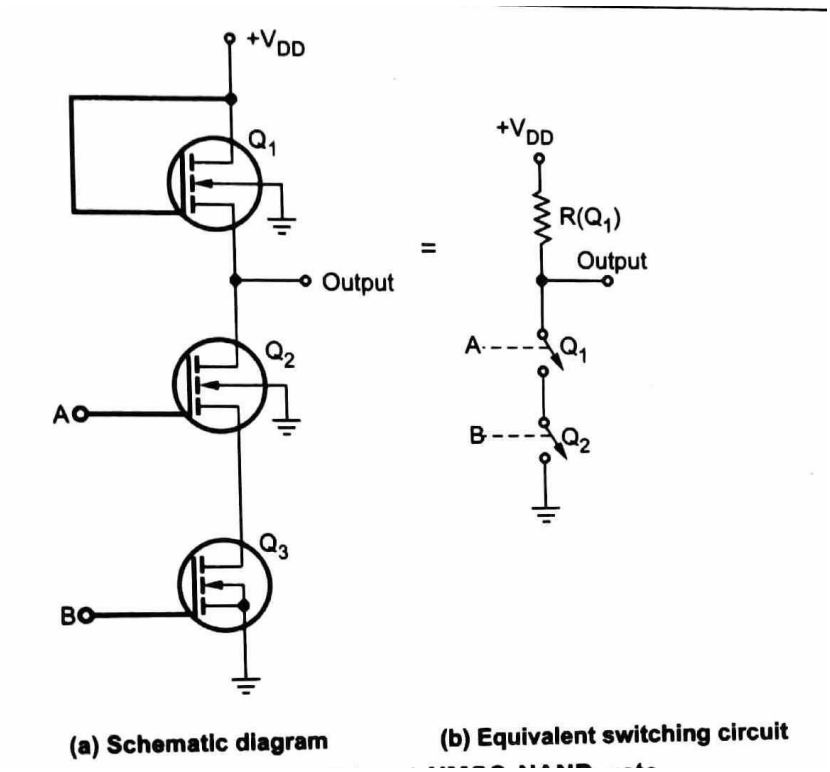
a) OR
b) NAND
c) AND
d) NOR

30 | The DTL, TTL, ECL and CMOS families of digital ICs are compared in the following 4 columns. Which option is correct? | 2 | 5 | 2

	(P)	(Q)	(R)	(S)
Fanout is minimum	DTL	DTL	TTL	CMOS
Power consumption is minimum	TTL	CMOS	ECL	DTL
Propagation delay is minimum	CMOS	ECL	TTL	TTL

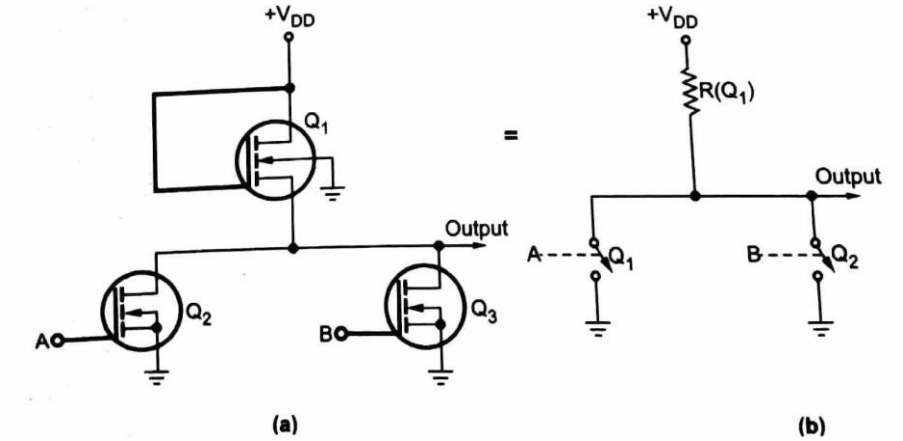
a) P
b) Q
c) R
d) S

31 | The figure (a) shows the schematic diagram and figure (b) shows the equivalent switching circuit of a gate using NMOS. The circuit represents a | 2 | 5 | 3



(a) Schematic diagram **(b) Equivalent switching circuit**

a) OR
b) NAND
c) AND
d) NOR

32	The figure (a) shows the schematic diagram and figure (b) shows the equivalent switching circuit of a gate using NMOS. The circuit represents a  a) OR b) NAND c) AND **d) NOR**	2	5	3
33	How many address bits are needed to operate a 2K * 8-bit memory? a) 10 **b) 11** c) 12 d) 13	2	5	2
34	What is the bit storage capacity of a ROM with a 1024 × 8 organization? a) 1024 b) 4096 c) 2048 **d) 8192**	2	5	2
35	Suppose that a certain semiconductor memory chip has a capacity of 8K × 8. How many bytes could be stored in this device? a) 8,000 b) 65,536 **c) 8,192** d) 64,000	2	5	2